REMARKS

Claims 1-20 are pending in the application. In view of the comments herein, reconsideration and a withdrawal of the Examiner's rejections is hereby respectfully requested.

1. Brief Description of the Drawings.

The Examiner has pointed out that the specification does not include a brief description of the drawing. Applicant has amended the specification to include a heading -- Brief Description of the Drawing Figure -- and a paragraph describing the drawing. Applicant has reviewed the specification and has inserted appropriate headings, and corrected spellings, as indicated above. A substitute specification is provided herewith which incorporates the amendments to the specification listed above. No new matter has been introduced.

2. The Objections to Claim 12.

Claim 12 stands objected to as being in improper form. Claim 12 has been amended to depend from claim 1 in order to conform to the claim requirements. Claim 12 is now believed to overcome the objection.

3. The Examiner's 102(b) rejection of Claims 1-11 and 13-20 over U.S. Patent 4,720,324 ("Hayward").

Claims 1-11 and 13-20 stand rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. 4,720,324 ("Hayward"). This rejection is respectfully but

strenuously traversed and reconsideration and a withdrawal of the rejection are hereby respectfully requested.

Applicants' present invention is distinguishable over Hayward and should be patentable. The Examiner contends that claim 1 of the present invention discloses the invention asserting that Hayward teaches a process for producing a solderable surface and a functional surface on a dielectric substrate. The Examiner states that, in Hayward, the dielectric substrate is provided with copper structures (tracing), and that solderable surfaces are created by deposition of a tin alloy by chemical reduction (electroless plating). The Examiner further asserts that *a covering mask (resist) is placed over solderable areas leaving functional areas (pads) exposed*, that functional surfaces are created by chemical reduction (plating), and that after formation of pads and plated holes, the masking material (resist) is removed (col. 2, line 65 - col. 3, line 10); that the solderable material comprises gold, nickel, palladium or tin (col. 5, lines 27-43); that a solder mask is applied and functional areas are formed (col. 5, line 35 - col. 6, line 20); that gold may be applied over the base layer of nickel (col. 6, lines 44-46); that the tin layer may be removed before formation of the functional area by acid etching (col. 5, lines 58-68); that the covering mask may comprise a photo-resist which is applied and developed by exposure or may be screen printed; and that a first mask (130) may be applied before forming the solderable areas with necessary areas left bare (exposed), (col. 4, line 38 - col. 5, line 16).

The applicants' present invention is distinguishable over Hayward and is not disclosed, taught or suggested by that reference. Applicants' present invention provides a novel process for producing at least one solderable surface in selected solder regions and at least one functional surface in functional regions differing from the soldering regions on the surfaces of copper structures on printed circuit carriers. As set forth in claim 1, the process of the applicants' present invention (see the specification at page 5) involves the following steps:

(a) first, a dielectric substrate is provided with copper structures;

(b) then, the solderable surfaces (5) are created by depositing a solderable layer of metal;

(c) then, a covering mask is formed that covers the solder regions (2) and leaves the function regions (4) uncovered;

(d) subsequently, the functional surfaces (7, 8) are created in the function regions and

(e) the covering mask is cleared off.

Following the steps of the present process, a board is produced, which shows solderable surfaces and functional (e.g. bondable) surfaces at the same time (page 5, lines 2-3), wherein the functional surfaces in the function regions are formed in step (d). The solderable surface of the applicants' invention may be made to receive surface mount pads (terminal pads), wherein these pads are situated in solder regions, and made of tin/lead for example. In contrast, the term "functional surface" of the applicants' invention relates to surfaces with a technical function, which are built up

in function regions. The functional surface serves preferably as a bondable surface in a function region. In principle, the functional surfaces can also be suited for producing electrical contacts that can be opened (e.g. keypads and edge connector contact areas) (see the applicants' specification at page 5, lines 16-18).

Hayward discloses a process for the manufacture of a circuit board. In Hayward, the end product contains a surface-mounted component at a solderable surface in a solder region (160, Fig. 2d) and circuit traces made of copper in a function region (140, Fig. 2c). Furthermore, the Hayward product contains edge connectors, e.g. made of gold (col. 6, lines 44-46), which may be considered to represent a function area with a functional surface. Hayward, however, does not disclose the applicants' novel process. The steps disclosed in Hayward are not the same as in the present invention, and therefore applicants' present invention should be patentable.

When Hayward is considered for what it fairly discloses, it does not teach, suggest or disclose the applicants' present invention. Turning to Hayward, the circuit board is formed by applying a plating resist (130) with the desired circuit pattern (Fig. 2b). The exposed areas are the areas (140), (150) and (160). (col. 4, lines 63-66) Area (140) will become a circuit trace. Area (150) will become a plated through hole and the area (160) will become a surface mounted terminal pad (col. 4 line 63 – col. 5 line 6). The layer (170) within these areas is then coated with a metallic material

(172) that may be used as an etch resist and is at the same time compatible with solder (col. 5, line 27-34; Fig. 2c). In the Hayward method, *a second plating resist (180) is applied*, leaving only the surface mount pads (terminals) exposed (Fig. 2d). Unlike Hayward, in the present invention, at this stage of the process, the function areas are exposed to create the functional surfaces of nickel/gold for example. According to Hayward, the surface mount pads are then electroplated with a thick coating (190) of tin/lead. The plating resists are then chemically stripped and the exposed and unwanted copper is chemically etched away (Fig. 2e/2f). After applying further steps, the resulting board (Fig. 2h) contains surface mounted components (210) at the described surface mount pads (Fig. 2g), circuit traces and plated through holes. The circuit traces and the plated through holes are made of copper (114, 120, 170) (col. 5, line 35 – col. 7, line 29).

The Examiner's rejection must fail. Contrary to the Examiner's statement (page 3, lines 4-5), the covering mask of Hayward (180), unlike the process of the present invention, is not placed over the solderable areas, because the exposed areas (160) are built up to a solder area with a solderable surface (tin/lead - layer 190), made for terminal pads (col. 5, lines 5-6). Therefore, if Hayward were to cover the solderable areas, as is done in the applicants' present invention, Hayward would not be functional or be able to achieve its intended purpose, since the coating (190) could not be applied.

In addition, Hayward fails to suggest or disclose a process of creating its functional layers (even as edge connectors, e.g. made of gold). Contrary to the Examiner's assertion on page 3 of the Office Action, Hayward does not disclose the removal of Sn layer *before formation of a function area*. The process disclosed and claimed by the applicant specifies "functional" and "solderable" surfaces, and describes function regions and solder regions. Hayward, when viewed for what it fairly discloses, for these additional reasons, fails to anticipate or suggest the process disclosed and claimed as the applicants' present invention. Applicants' present invention as recited in the pending claims, provides a novel method which has the benefit of conserving resources and being economical in that a functional surface is only formed in those regions on the surface of the circuit carriers in which bonded connections with the components are to be formed, whereas in the regions in which soldered connections are to be formed, an inexpensive solderable layer of metal is deposited. Therefore, the applicants' present invention has advantages in facilitating the reduction of the waste ratio with respect to solderability over the prior methods.

Hayward merely mentions a functional surface, such as edge connectors, but, as previously mentioned, does not suggest how to produce such a surface. Hayward appears to mention production of solderable surfaces in solder regions but does not disclose the claimed process of the present invention, which subsequently forms step-by-step solderable surfaces in solder regions and functional surfaces in function regions.

For the above reasons, the applicants' present invention is not disclosed by Hayward, nor is it taught or suggested. Applicant hereby respectfully requests reconsideration and withdrawal of the Examiner's rejection with respect to Hayward.

4. The Examiner's 102(b) rejection of Claims 1-3, 6-11 and 13-19 over U.S. Patent 4,104,111 ("Mack").

Claims 1-3, 6-11 and 13-19 stand rejected as being anticipated by U.S. Patent 4,104,111 ("Mack"). This rejection is respectfully but strenuously traversed and reconsideration and a withdrawal of the rejection are hereby respectfully requested.

Applicants' present invention is distinguishable over the Mack reference. Mack relates to a process of manufacturing printed circuit boards (PCB's), in which, at the end of the process, the circuit board contains a covered area (14), which is a circuit trace, and a terminal pad area (15) into which a component lead will be inserted (col. 6, lines 35-37). In Mack, edge connectors, e.g. made of gold, may be created (col. 8, lines 24-26). While it appears the Examiner may consider those edge connectors to represent a function area with a functional surface according to the present invention, there is no process disclosed by Mack, as to the generation of these functional surfaces.

Mack fails to disclose the process steps as claimed in the applicants' present invention. The steps of the Mack process are not the same as those disclosed and claimed as of the applicants' present invention. Accordingly, applicants' invention should be patentable over Mack, as there are appreciable differences. The Mack

process of manufacturing printed circuit boards starts with depositing copper onto a pre-drilled copper-clad substrate, then applying plating resist in the pattern desired. Circuit traces are built up to the desired thickness by electroplating the desired metal, copper for example, onto the circuit pattern. Over the copper, a plating of durable, chemically passive metal such as tin/nickel is next plated which serves as an etching resist in later steps and provides a desirable surface finish for the copper (col. 4, lines 47-55). The next applied plating resist leaves the terminal pads (15) and the connector areas exposed (col. 7, lines 29-31) in order to apply a final electroplating of tin/lead onto the terminal pads (15) and the connector areas (col. 4, lines 55-59). During this operation, the area (14) is covered by the plating resist (col. 7, lines 29-35). The plating resists are then chemically stripped and the remaining exposed copper is etched away. Finally a permanent solder mask (21) is applied (col. 8, lines 26-28) leaving the area (14) covered and having a ***tin/lead coated area (15) uncovered*** (Fig. 2(i)).

Based on the description above from Mack, and referring to the Examiner's comments in par. 4, of the Office Action, it appears that the Examiner has misconstrued what is actually disclosed in Mack. In order to support the rejection of the present invention over Mack, the Examiner states that in Mack, a covering mask is placed over the solderable areas, leaving the *functional areas* exposed. But in fact, what Mack actually discloses is that *the covered area is area (14), which is specified as a circuit trace* (col. 6, lines 35-36). This means that this area (area (14)) is not a

solder region. On the other hand, connector areas are mentioned, which may be function areas. But a method to their formation is neither shown nor specified in the Mack reference. Contrary to the Examiner's assertion, the *exposed area (15)* would refer to a *solder region* (terminal pad area (col. 6, lines 36-37)) rather than to a function region. Hence the solderable surface, unlike in the present process, is not covered during the process of Mack. In the present invention, the ***solderable surface (5) is covered***. (See Fig. 1, steps C-E).

Furthermore, the Examiner's statement on page 4, lines 3-4 regarding Mack also appears to be misplaced. Contrary to the citation in col. 7, lines 36-66 to which the Examiner refers, Mack does not appear to disclose in the specification at all, a functional surface created by chemical reduction. In addition, in Mack, the function areas (edge connectors) are generated parallel to the solder areas (col. 4, lines 46-61; col. 7, lines 3-5, 29-31) and are finally plated with gold for example (col. 8, lines 24-26). Differentiation of the solder and these function areas by process is not disclosed by Mack.

For these reasons, Mack does not disclose the applicants' presently claimed invention, nor is the present invention obvious in view of Mack. Mack provides a process to produce a board with function areas and solder areas, whereas function areas (edge connectors) are first generated parallel to the solder areas (col. 4, lines 46-61; col. 7, lines 3-5, 29-31) and are finally plated with gold for example (col. 8, lines

24-26). In Mack, differentiation of the solder and function areas by process is not disclosed. Mack therefore, fails to disclose, teach or suggest the claimed process of the present invention, as the process of the present invention subsequently forms step by step solderable surfaces in solder regions and functional surfaces in function regions. For these additional reasons, the subject matter of the present invention is not anticipated by, nor is it obvious to one of ordinary skill in the art at the time the invention was made. Applicant hereby respectfully requests reconsideration and withdraw of the Examiner's rejection with respect to Mack.

5. The Examiner's 102(e) rejection of Claims 1, 3-11, 14, 15, 19 and 20 over U.S. Patent 6,242,078 B1 ("Pommer").

Claims 1, 3-11, 14, 15, 19 and 20 stand rejected as being anticipated by U.S. Patent 6,242,078 B1 ("Pommer"). This rejection is respectfully but strenuously traversed and reconsideration and withdraw of the rejection are hereby respectfully requested.

Applicants' invention is distinguishable over Pommer. Pommer relates to a method and apparatus for providing a high density printed circuit substrate. The substrate in Pommer comprises a dielectric layer, which will be provided with circuit traces. The end product of Pommer, however, is completely different in comparison to the end product of the process according to the present invention. Moreover, the starting materials in both cases are different, the present invention starting with a dielectric substrate, and Pommer a base laminate (50). For this reason alone, the

claimed process of the present invention has to be different from the one disclosed in Pommer, and hence the subject matter as claimed in the present patent application is novel over Pommer.

There are yet additional reasons why Pommer still does not teach, suggest or disclose the applicants' present invention. In Pommer, after providing a base laminate (50) with a via opening (52a, 52b), the process starts with the deposition of a first (54) and a second conductive layer (56) (col. 4, lines 1-46). Then, a plating resist (58) is applied (Fig. 3D and 3E), leaving the via openings (52a, 52b) and some portions at the second conductive layer exposed (col. 5, lines 1-8). An additional layer of conductive material (60), e.g. copper, is deposited to facilitate fine line geometry circuits (col. 5, lines 13-17). In Fig. 3H, the plating resist and the different conductive layers under it are removed to form the substrate (26), where only a single kind of solderable or bondable surfaces exists. With respect to Fig. 2 of Pommer, in the detailed description (col. 3, lines 56-65), there is mentioned a substrate (26) containing a surface having pads, routing traces, etc. An integrated circuit (22) may be mounted to this substrate by way of flip chip solder connections. Alternatively, the integrated circuit may also be mounted to this substrate with bond wires.

In contrast to the present invention, in Pommer, there are ***not solder regions and function regions*** on the dielectric substrate ***at the same time***. Therefore, the end product of the present invention is not the same as described by Pommer. In fact, the

Pommer process ends up with a circuit substrate, which is in principle *the base material* for the process according to the present invention. Therefore, Pommer merely provides teaching of a starting material, after which, the applicants' process would be applied in order to carry out the steps of the present invention. Pommer discloses a method and apparatus for providing an electrical substrate. The present invention claims a method for producing functional and solderable surfaces on circuit carriers (i.e. substrates). The starting material of the present invention, i.e. a substrate, is the type of article that the Pommer reference seeks to produce. The present invention applies its method steps to produce solderable and functional surfaces on a substrate. Therefore, for these reasons, Pommer cannot teach, suggest or disclose the applicants' present invention. When the Pommer reference is considered for what it fairly discloses, one does not find the method steps claimed in the applicants' invention.

Applicants' claimed process is further distinguishable over Pommer. With respect to the Examiner's comments in paragraph 5 of the office action, the Examiner makes a reference on page 4, lines 19-20 of the Office Action, that *a covering mask would be placed over the solder areas leaving function areas exposed* (col. 5, lines 1-12). In view of what is fairly disclosed in Pommer (see e.g. col. 3, lines 43-65), there does not appear to be solder ***and*** function areas on the substrate present at the same time. Therefore, it does not appear that the covering mask referred to by the Examiner could indeed be placed over the solder areas leaving function areas

exposed. For these additional reasons, Pommer is still yet deficient in providing a disclosure, teaching, or suggestion of the applicants' present method. As has been explained before, however, there are no solder and function areas on the substrate present at the same time. Therefore, the Examiner's contention that Pommer teaches or discloses placing a covering mask over solder areas and leaving function areas exposed, does not appear to be supported by Pommer, and is, in fact, contradictory to what Pommer actually discloses (see col. 3, lines 43-65).

Pommer does not refer to the same subject matter as claimed in the present patent application, and there is no suggestion in Pommer as to forming selectively solder and function regions as claimed in the present patent application. For the above reasons, the applicants' claimed method is novel over Pommer, and should be patentable. Reconsideration and withdraw of the Examiner's rejection of claims 1, 3-11, 14, 15, 19 and 20, with respect to Pommer, is hereby respectfully requested.

The prior art made of record and not relied upon, for the same reasons as those set forth herein, also fails to teach, suggest or disclose the applicants' present invention.

CONCLUSION

For the reasons set forth above, applicants' present invention, as recited in the pending claims, is distinguishable over the cited patent references, and is not taught, suggested or disclosed thereby. Applicants' invention provides a novel method and

circuit carrier and should be patentable. Reconsideration and early allowance of the pending claims is earnestly solicited.

The Commissioner is authorized to charge any additional fees which may be required to Patent Office Deposit Account No. 05-0208.

Respectfully submitted,
Harding, Earley, Follmer & Frailey
Attorneys for Applicant

Frank J. Bonini, Jr.
Registration No. 35,452
P.O. Box 750
Valley Forge, PA 19482-0750
Telephone: 610/935-2300

Date: 3/6/03

In re Application of
Christian Wunderlich et al.
Serial No.: 09 937,363
Filed: September 21, 2001
For: PROCESS FOR THE PRODUCTION OF SOLDERABLE AND FUNCTIONAL SURFACES ON CIRCUIT CARRIERS

Honorable Commissioner
of Patents and Trademark
Washington, DC 20231

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I hereby certify that this correspondence and the documents referred to as attached therein are being deposited today with the United States Postal Service as first-class postage-prepaid mail in an envelope addressed to: Assistant Commissioner of Patents and Trademarks, Washington, DC 20231.

3/6/03
Date:

Frank J. Bonini, Jr.
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The Commissioner is hereby authorized to charge any additional fees which may be required by this paper and during this pendency of this application to Account 05-0208.

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Reg. No. 35,452

SIR:

APPENDIX OF AMENDED CLAIMS MARKED UP TO SHOW CHANGES

12. (Amended) Process according to claim 1 [one of the preceding claims], wherein the covering mask is formed by means of a screen printing process.